ABSTRACT OF THE DISCLOSURE

Planarized STI with minimized topography is formed by selectively etching back the dielectric trench fill with respect to the polish stop film prior to removing the polish stop film. Embodiments include etching back a silicon oxide trench filled to a depth of about 200 Å to about 1,500 Å, and then stripping a silicon nitride polish stop layer leaving a substantially planarized surface, thereby improving the accuracy of subsequent gate electrode patterning and reducing stringers.